IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Yi Ding		
Assignee:	Mosel Vitelic, Inc.		
Title:	Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions		
Application No.:	Unassigned	Filing Date:	Filed Herewith
Examiner:	Unassigned	Group Art Unit:	Unassigned
Docket No.:	M-15241 US		

San Jose, California
July 30, 2003

Mail Stop Patent Application
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required. If a fee is required for this Information Disclosure Statement, please charge the fee to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15241 US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	Filed Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,402,371	28 Mar. 1995	Ono			
	AB	5,856,943	5 Jan. 1999	Jenq			
	AC	6,057,575	2 May 2000	Jenq			
	AD	6,130,129	10 Oct. 2000	Chen			
	AE	6,134,144	17 Oct. 2000	Lin et al.			
	AF	6,171,909	9 Jan. 2001	Ding et al.			
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	AI	6,326,661	4 Dec. 2001	Dormans et al.			
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	AK	6,365,457	2 Apr. 2002	Choi			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Shirota, Riichiro "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend," February 2000, Nonvolatile Memory Workshop in Monterey, California, pages 22-31.
	AM	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pages 604-606.
	AN	Wu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.
	AQ	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate Fro High-Density and High Performance Device," 1985 IEEE, 635-638.
	AP	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 49-50.
	AQ	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.
	AR	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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	Filed Herewith	Unassigned

U.S. Patent Documents

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	AS	6,437,360	20 Aug. 2002	Cho et al.			
	AT	6,438,036	20 Aug. 2002	Seki et al.			
	AU	6,486,023	26 Nov. 2002	Nagata			
	AV	6,541,324	1 Apr. 2003	Wang			
	AW	2002/0064071 A1	30 May 2002	Takahashi et al.			
	AX	2002/0197888 A1	26 Dec. 2002	Huang et al.			
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	BA	6,518,618	11 Feb. 2003	Fazio et al.			
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	BC	6,414,872	2 Jul. 2002	Bergemont et al.			

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	BD	Spinelli, Alessandro S., "Quantum-Mechanical 2D Simulation of Surface-and Buried-Channel p-MOS,"2000 International Conference on Simulation of Semiconductor Processes and Devices: SISPAD 2000, Seattle, WA September 6-8, 2000
	BE	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technolgy Scalabe to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4
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	BG	Van Duuren, Michiel et al., "Compact poly-CMP Embedded Flash Memory Cells For One or Two Bit Storage," Philips Research Leuven, Kapeldreef 75, B3001 Leuven, Belgium, pages 73-74.
	BH	
	BI	
	BJ	

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